a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit; and

a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

REMARKS

The Office Action dated December 3, 2002, has been received and carefully noted. The period for response having been extended from March 3, 2003 to April 3, 2003, by the attached Petition for Extension of Time, the amendments made herein and the following remarks are submitted as a full and complete response thereto.

Applicant appreciates the allowance of claims 22-37. In addition, Applicant also appreciates the indication of allowable subject matter within claims 20, 21 and 39-42. Claims 19, 38 and 43-47 have been amended. Applicant submits that no new matter has been added by the amendment made herein. Therefore, claims 19-47 are pending in the present application, and Applicant submits claims 19, 38 and 43-47 for reconsideration.

Claims 19, 38 and 43-47 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kim et al. (U.S. Patent No. 5, 789,948, hereinafter "Kim"). Applicant respectfully submits that each of claims 19, 38 and 43-47 recite subject matter which is neither disclosed nor suggested in the cited prior art.

Claim 19 recites an input buffer circuit having a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals, and includes a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit. In addition, the input buffer circuit includes a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal, and includes a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

Claim 38 recites an input buffer circuit having a differential amplifier circuit, a first circuit, a second circuit and a control circuit. The differential amplifier circuit receives first and second input signals and generates an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply, for receiving the first input signal. The control circuit is coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal while isolating the

other one of the first circuit and the second circuit from the first power supply or the second power supply.

Claim 43 recites an input buffer circuit having a differential amplifier circuit, a first circuit, a second circuit and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit. The control circuit selectively enables one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

Claim 44 recites an input buffer circuit having a differential amplifier circuit, a first circuit, a second circuit and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit. The control circuit selectively isolates one of the differential amplifier circuit and

the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

Claim 45 recites an input buffer circuit having a differential amplifier circuit, a first circuit, a second circuit and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit. The control circuit selectively enables one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

Claim 46 recites an input buffer circuit having a differential amplifier circuit, a first circuit, a second circuit and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the

second power supply, for receiving the first input signal and generating a single output signal to the first circuit. The control circuit selectively enables one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

Claim 47 recites an input buffer circuit having a differential amplifier circuit, a first circuit, a second circuit and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit. The control circuit selectively isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

Accordingly, the present invention provides an input buffer circuit of a semiconductor integrated circuit device, wherein the input buffer circuit receives a small amplitude signal. Therefore, the present invention results in the advantage of having an input buffer circuit with reduced power dissipation.

It is respectfully submitted that the prior art fails to disclose or suggest the element of a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply, in the presently pending claims, and therefore fails to provide the advantages which are provided by the present invention.

Kim discloses a sense amplifier having a voltage level shifter for shifting a voltage level of data from a memory cell in response to a sense amplifier enable signal. The sense amplifier of Kim also includes a current mirror type sense amplifying stage for amplifying the level-shifted data from the voltage level shifter to full range in response to the sense amplifier enable signal, and a driver means for driving the amplified data from the current mirror-type amplifying stage.

Applicant respectfully submits that each and every element recited within claim 19 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the input buffer circuit having at least a control circuit as recited in the present application is clearly distinct from that which is illustrated in Kim. It is submitted that Kim fails to disclose or suggest a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply. Specifically, claim 19 has been amended to clarify that one of a

differential amplifier circuit and a second circuit is enabled while isolating (disabling) the other one of the differential amplifier circuit and the second circuit.

As for claims 38, 43-47, it is submitted that each of these claims has also been amended to clarify the limitations recited therein. In particular, each of claims 38, 43-47 has been amended to recite that one of a differential amplifier circuit and a second circuit is enabled while isolating (disabling) the other one of the differential amplifier circuit and the second circuit.

Applicant submits that although Kim discloses a conventional paired current mirror-type sense amplifier having N-MOS transistors N1-N9, and P-MOS transistors P1-P7, it is respectfully submitted that Kim nevertheless fails to disclose or suggest that one of a differential amplifier circuit and a second circuit is enabled while isolating (disabling) the other one of the differential amplifier circuit and the second circuit. Accordingly, Applicant respectfully submits that Kim fails to disclose or suggest each and every element recited within claims 19, 38 and 43-47 of the present application.

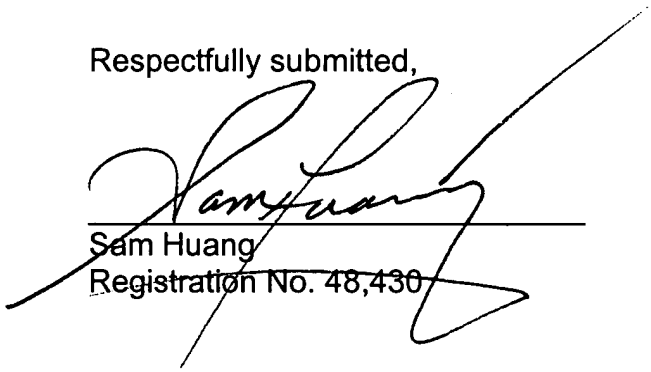
In view of the above, Applicant respectfully submits that claim 19, 38 and 43-47, ach recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully requests that claims 19, 38 and 43-47 be found allowable along with allowed claims 22-36 and allowable claims 20, 21 and 39-42, and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by

telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to Attorney Docket number 108075-00056.

Respectfully submitted,



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Enclosures: Marked-Up Copy of Amended Claims
Petition for Extension of Time (one month)

MARKED-UP COPY OF AMENDED CLAIMS

19. (Twice Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal[, wherein the control circuit isolates a disabled] while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

38. (Twice Amended) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit, coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal[, wherein the control circuit isolates a disabled] while isolating the other one of the first circuit and the second circuit from the first power supply or the second power supply.

43. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

44. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

45. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal[, wherein the control circuit isolates a disabled] while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

46. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

47. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit; and

a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.